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DESIGN OF 7NM FINFET WITH HIGH-K DIELECTRIC OXIDE AND METAL GATE (HK-MG) USING ASHBY'S MATERIAL SELECTION (AMS) APPROACH

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Abstract

Using non-planar (3D) transistor architectures like FinFETs and Gate-all-around (GAA) FETs is a major advancement in the electrical industry. Multiple considerations have shown that 3D transistors are replacing 2D planar transistors. Short channel effects may be mitigated by using 3D transistors to adjust channel area. However, silicon dioxide (SiO_2) dielectric performance limits device scaling. FinFETs using HK-MG materials can better manipulate channel electrons, improving device performance. In FinFET technology, HK-MG materials are compatible with traditional manufacturing methods, meeting the need for a replacement to SiO2. Hafnium and Titanium oxides are promising high-k dielectrics for submicron electronics. This study uses Ashby's methods to choose high-k metal gate (HK-MG) materials for FinFETs. The goal is to simulate energy band-gap, electric field distribution, charge density, and surface potential to prove these materials can replace SiO2.FinFET with HK-MG improves band-gap Energy (Eg) in addition to Electric Field Density, Surface Potential and Charge Density Distribution. With the use of High-k materials the corresponding bandgap energy is reduced. With Si. Ge, GaAs, InN and GaN the Eg (eV) was reduced to about 0.613eV, 0.08eV, 0.879eV, 1.932eV and 1.148eV respectively. As a result, GaAs, InN, and GaN as metal gate (MG) materials are more appropriate candidates than classic Si materials. High-k dielectric oxide (HK) materials and Metal Gates (MG) are examined for energy band-gap, electric field distribution, charge density, and surface potential in this work. Semiconductors with better electron mobility than silicon are better for high-frequency applications. GaN's high mobility and power density, which dissipates heat from tiny components, are noteworthy.

Keywords: Band Gap Energy, Charge Distribution, Electric Field Distribution, Non-Planar FETs, Surface Potential.

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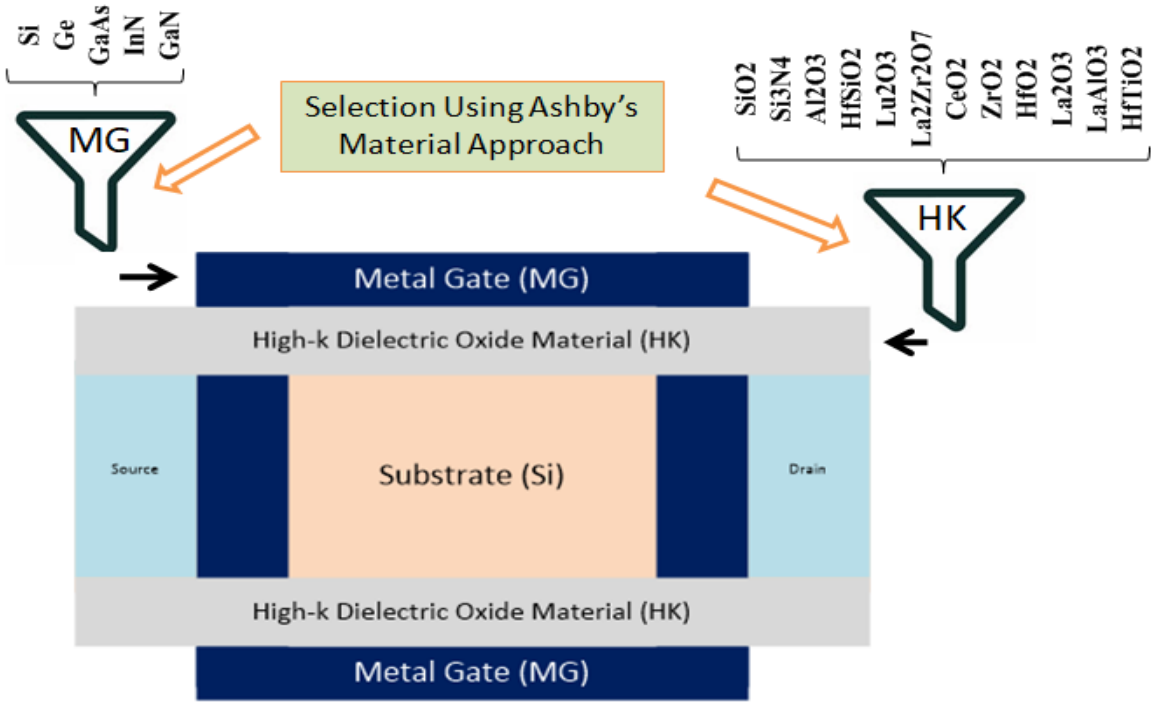

Graphical Abstract: FinFET Device utilizing HK-MG using AMS

1. INTRODUCTION

Semiconductor devices are widely used in every electronic circuit. The journey embarked with the invention of vacuum tubes by John A. Fleming in 1904 which works on the concept of thermionic emission. Due to its bulky nature, the vacuum tubes were replaced by Bipolar Junction Transistors (BJT) in 1947 by William Schockley, John Bardeen and Walter Brattain at Bell's Laboratory. In simple terms a BJT is a combination of unipolar junction diodes capable to amplify and switch electronic signals. Later on in 1953 a working practical Junction Field Effect Transistor (JFET) was built by George F.Dacey and Ian M.Ross, named on its working principle which illustrates that the switching activity of the gate is accomplished by the electric field created across the oxide junction. In 1950 Mohammed Atalla experimentally presented a silicon oxide on a silicon surface that neutralizes the surface states and lead to the invention of Metal Oxide Semiconductor FET (MOSFET). A basic MOSFET comprises of a "metal" as gate material with source and drain regions formed by implanting donor impurities, silicon di-"oxide" as insulator and silicon "semiconductor" as substrate. In terms of power consumption and high density, a MOSFET supersedes BJT and FET, but is limited by power dissipation which can be overcome by using Complementary MOS (CMOS). A CMOS device is widely used in integrated circuits (IC) often used in digital logic circuits.

With continuously scaling down of transistor dimensions, results in short channel effects (SCEs) like leakage current, gate capacitance, threshold voltage roll-off, Drain Induced

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Barrier Lowering (DIBL), drain punch through etc[1]. To meet the consumer market in fulfilling the Power, Performance, Area (PPA) requirement the semiconductor devices are continuously scaled down in-terms of its horizontal and vertical dimensions. This down-scaling trend followed the Moore's Law postulated by Gordon Moore in 1965 which states that the number of transistors in an IC doubles every two years. Based upon this theory, International Technology Roadmap for Semiconductors (ITRS) serves as a ground plan for the semiconductor companies to come up with ways like introducing multi-core devices, reducing supply voltages, alternative materials, advanced device technologies etc, to continuously maintain the Moore's theory [2]. The journey in scaling the transistor dimensions started with 10 micro-meter (um) to current trend with 5nm technology node. Below 45nm the MOSFETs experienced process variations, reduced reliability, device defects and short channel effects (SCE) [1]. These limitations can be overcome with use of High-k oxide materials, metal gate materials [3] and non-classical device structures like Fin Shaped FETs (FinFET).

In a basic MOSFET, the silicon dioxide (SiO2) layer is formed by oxidizing the silicon substrate thus forming a uniform and stable oxide layer. For decades, silicon dioxide (SiO2) has been employed as a gate oxide material. The thickness of the SiO2 gate dielectric has gradually dropped as the size of MOSFETs reduces, increasing gate capacitance (per unit area) and driving current (per device width), thereby deteriorating device performance. Tunneling leakage currents grow dramatically when the thickness scales below 32 nm, resulting in excessive power consumption and lower device dependability. By replacing the silicon dioxide gate dielectric with a high- material, the gate capacitance can be enhanced without the accompanying leakage consequences. Earlier above 45nm regime, manufactures preferred poly-silicon gate over metal gates due to the fact that the operating voltages for polysilicon is from 2-5V. Over the course, as the technology node is shrinked, resulting in subsequent decrease in the operating voltages, channel length, channel width etc., the manufactures resumed back to metal gate to cope up with the continuous down-scaling of device structures. One of the main reason for this recommence is the higher threshold voltage and higher conductivity of metal gates as the poly-silicon gate layers cannot be shrink further alone to improve the speed[4] which can be used in high speed low power applications[5],[6].

Below 45nm regime, to improve the performance and reduce the SCEs of the planar MOSFET structure, alteration in terms of metal gate (MG) material and high-k (HK) dielectric oxide material is one such approach. Intel implemented an alternative integration scheme subsequent to their adoption of high-k dielectric materials in lieu of oxide materials, during the development of their 45nm node CMOS technology. This integration process was commonly referred to as "gate last," "RMG" (Replacement Metal Gate), or "damascene." The crucial procedural stage involved in this integration pertains to the substitution of the SiO2/poly-Si gate subsequent to the source/drain activation anneal with a HK/MG structure featuring gate materials tailored for pMOS and nMOS transistors [7]. Furthermore below 32nm regime, the alterations made for the materials have null affect in improving the MOSFET device performance. This lead to the new class of advanced technologies broadly termed as non-classical/non-planar device structures

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like FinFET. The total drive current and reduction in SCEs are proportional to the number of fins. Also, researchers in [8] proposed the use of high k-metal gate structure to significantly improve the gate-to-channel capacitance and leakage current in comparison with the traditional silicon dioxide (Sio2) material. Researchers in [9], [10] focused upon improving the electron mobility which is related to the gate length of the device showing significant reduction in SCEs and leakage currents. Researchers in [11] concludes a significant improvement in operational capabilities through the utilization of linear high-k along with reduced power dissipation per gate, thus achieving a greater scaling for improved packing density which necessitates a reduction in gate oxide thickness relative to channel length. The aforementioned initiative facilitated the reduction in size of logic devices and the production of device featuring dielectric films with sub-nanometer thickness.

Due to the abundance of available materials, it is crucial to carefully choose the optimal material to improve the functionality of a device. The utilization of material selection approaches facilitates the identification of the trade-offs that exist between conflicting materials properties, thereby enabling the selection of the most optimal material for enhanced device performance. Ashby's approach is widely recognized as one of the most prevalent multi-objective decision-making (MODM) methodologies for material selection. This approach is favored due to its ability to optimize alternatives by prioritizing objectives. The Ashby approach outlines a means of characterizing materials suitable for achieving desired performance based on their specific attributes, including mechanical, electrical and thermal properties, in-addition with a process of screening is utilized to identify and shortlist attribute profiles [12].

2. MATERIAL AND METHODS

The state-of-design approach involves the use of a FinFET device structure operating in 7nm technology node. Using the predictive technology model (ptm) the device parameters used are illustrated in Table-1 for the heavily doped source/drain region and lightly doped gate region. The FinFET device is simulated using MUGFET simulation tool using high-k dielectric oxide materials metal gate materials. The best suited material(s) in terms of energy band gap and permittivity is determined using the application of Ashby's approach.

Table 1: 7nm FinFET Device parameters

Parameter	Value
Channel Length (L)	15nm
Channel Width (W)	7nm
Channel Height (H)	18nm
Oxide Thickness or thickness of the fin (t_{ox} / t_{fin})	6.5nm
Gate Length (L_g)	30nm
Source or Drain Length (L_s or L_d)	2nm
Source of Drain Overlap to Gate	0.2nnm
Source or Drain Doping concentration	3.00E+26 cm-3
Channel Doping	2.86.00E+25 cm-3

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Gate Voltage (V_g)	0.7V
Temperature	300k
Drain Voltage (Vd)	0.01 – 0.69V

2.1 FinFET Device Structure

A FinFET device is similar to the Tri-Gate (TG) FET, besides the use of a thick dielectric layer between the channel and top gate. This thick dielectric layer is often known as hard mask is responsible to inhibit an electric field and exerts parasitic inversion resistance[13]. The source and drain regions are oriented in 110- plane in contrast with the planar 100-plane orientation used for planar MOSFET. This 110-plane orientation is referred to as a fin, hence the name FinFET endowed with the requisite authorization from the regulatory entities responsible for overseeing the realm of patents [14]–[16]. In a FinFET transistor, the top gate has less control over the channel in contrast with the TGFET. A noted limitation of wielding the top gate in TGFET is that it limits the accumulation of electric field which can be overcome by the use of hard mask in FinFETs. Effectively the current drive in FinFETs is due to the side gates only expressed from equation (1) considering saturation region.

$$I_{ds} = \left(\frac{2H}{L}\right)\left(\frac{\mu C_{ox}}{2}\right)[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] \quad (1)$$

Where, Cox is the oxide capacitance, μ is the electron mobility, Vgs is the gate to source voltage, Vds is the drain to source voltage, Vt is the threshold voltage and H is the fin height of side gates.

As it can be noted from equation (1), the drain to source current of a FinFET varies in terms of the ratio expressed by $\left(\frac{2H}{L}\right)$ deferring from the ratio of planar MOSFET of $\left(\frac{W}{L}\right)$ in terms of divergence from the planar MOSFET (100-plane) towards the new plane as 110-plane illustrated in Figure1.

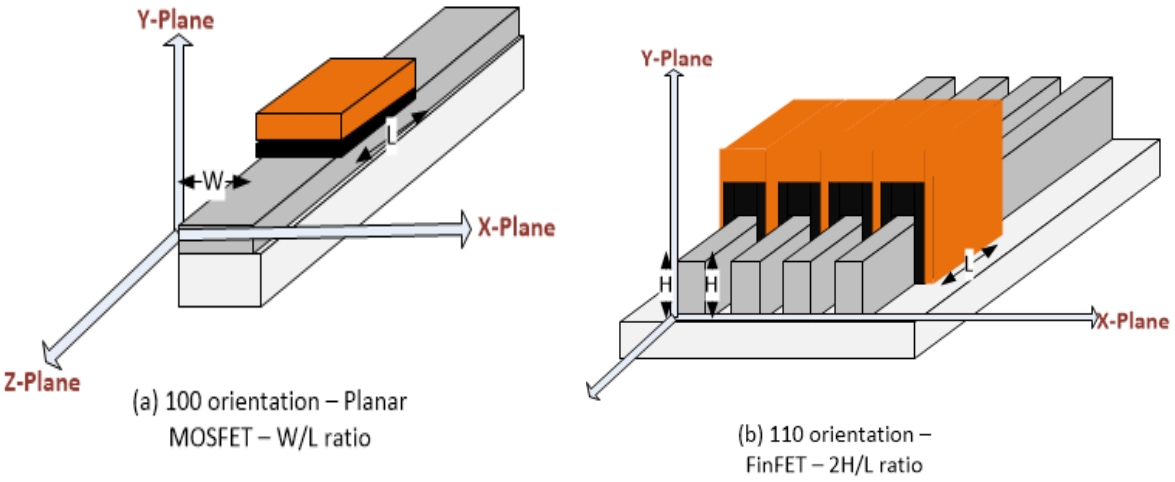

Figure 1: (a) Planar MOSFET 100 orientation, (b) Non-Planar FinFET 110 orientation.

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2.2 High-k Dielectric Oxide and Metal Gate (HK-MG) Materials

Moreover to achieve better performance, manufacturers and researches proposed the use of FinFET device structure alongside high-k dielectric materials as a replacement to the underlying oxide region and use of metal as gate material. The substitution of the gate dielectric composed of silicon dioxide with an alternative material introduces intricacy to the fabrication procedure. The process of oxidizing the underlying silicon leads to the formation of SiO2, which results in a uniform and conformal oxide layer with a high interface quality. Consequently, the focus of development endeavors has been directed towards the exploration of a material possessing a sufficiently high dielectric constant that can be seamlessly incorporated into a manufacturing process. Additional crucial factors to take into account are the alignment of the band to silicon, which has the potential to modify the leakage current, the morphology of the film, its thermal stability, the preservation of a high mobility of charge carriers in the channel, and the reduction of electrical defects in the film/interface.

Poly-Si exhibits moderate metallic properties; however, its carrier density is comparatively low, resulting in a depletion depth of only a few angstroms. In comparison, a metal of high quality exhibits a significantly greater carrier density and a shallower depletion depth of merely 0.5 Å. The depletion effect can be mitigated by substituting poly-Si with a conventional metal. Materials like Silicon Nitride (Si_3N_4), Aluminum Oxide (Al_2O_3), Hafnium Silicide ($HfSiO_2$), Lutetium Oxide (Lu_2O_3), Lanthanum Zirconate ($La_2Zr_2O_7$), Cerium Oxide (CeO_2), Zirconium Oxide (ZrO_2), Hafnium Oxide (HfO_2), Lanthanum Oxide (La_2O_3), Lanthanum Aluminum Oxide ($LaAlO_3$) and Hafnium Titanium Oxide ($HfTiO_2$) which exhibits higher dielectric constants than SiO_2 and moreover which can blend-in with the current fabrication processes.

Table 2 shows the Dielectric kappa (k) materials with respective energy band-gaps. When using high-k dielectric materials the performance of the device is drastically improved. For instance, a HfO_2 gate material 12nm film generates similar gate capacitance (C_g) and ON-current (I_{ON}) when using a 2nm film of SiO_2[4]. Properties of conventional metals like Germanium (Ge), Gallium Arsenide (GaAs), Indium Nitride (InN), Gallium Nitride (GaN) are illustrated in Table 2, which are incorporated alongside the above mentioned oxide materials signifying the state-of-design.

Table 1: High-k (HK) oxide materials

Oxide Material	Kappa (k value)	Band Gap (eV)
Silicon Dioxide (SiO2)	3.9	9
Silicon Nitride (Si3N4)	6.5	5.3
Aluminum Oxide (Al2O3)	9	7
Hafnium Silicide (HfSiO2)	11	6
Lutetium Oxide (Lu2O3)	15.95	5.5
Lanthanum Zirconate (La2Zr2O7)	16.4	4
Cerium Oxide (CeO2)	20	6
Zirconium Oxide (ZrO2)	23	6
Hafnium Oxide (HfO2)	24	6
Lanthanum Oxide (La2O3)	25	6

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Lanthanum Aluminum Oxide (LaAlO3)	30	5.6
Hafnium Titanium Oxide (HfTiO2)	60	5.7

Table 2: Metal Gate (MG) Materials

MG	k	Bandgap	Electron Affinity	Gate Work Function	Electron mobility
Si	11.7	1.12	4.05	4.6	1400
Ge	16.2	0.8	4	4.8	4000
GaAs	12.9	1.42	4.07	4.69	9000
InN	15.3	1.97	4.7	4.7	250
GaN	10.6	3.28	1.84	4.1	1500

2.3 Material Selection using Ashby's Approach

Due to the abundance of available materials, it is crucial to carefully choose the optimal material to improve the device performance. The utilization of material selection approaches offers an intuitive way of identifying the compromises that exist between competing materials properties, while also facilitating the identification of the most suitable material for enhanced device performance. Ashby's methodology is widely recognized as a prominent material selection approach. It provides a framework for identifying the optimal material for a given application based on its specific attributes, including mechanical, electrical, and thermal properties. A particular set of attributes is required by a design. The process of screening and ranking is utilized to identify and select attribute profiles. The material selection approach proposed by Ashby comprises a series of four sequential steps, as depicted in the accompanying chart in Figure. 2 The initial stage involves the formulation of design requirements for the structural component, which is based on its function, objectives, and constraints. The subsequent phase involves the reduction of the extensive range of options through the application of property constraints that eliminate materials which fail to satisfy the design specifications. The process of refining the selection is accomplished through the utilization of material indices and subsequent ranking of potential candidates according to their capacity to deliver optimal performance during the third step. The ultimate selection of material is determined by the comprehensive additional information of each shortlisted candidate, referred to as prime candidates.

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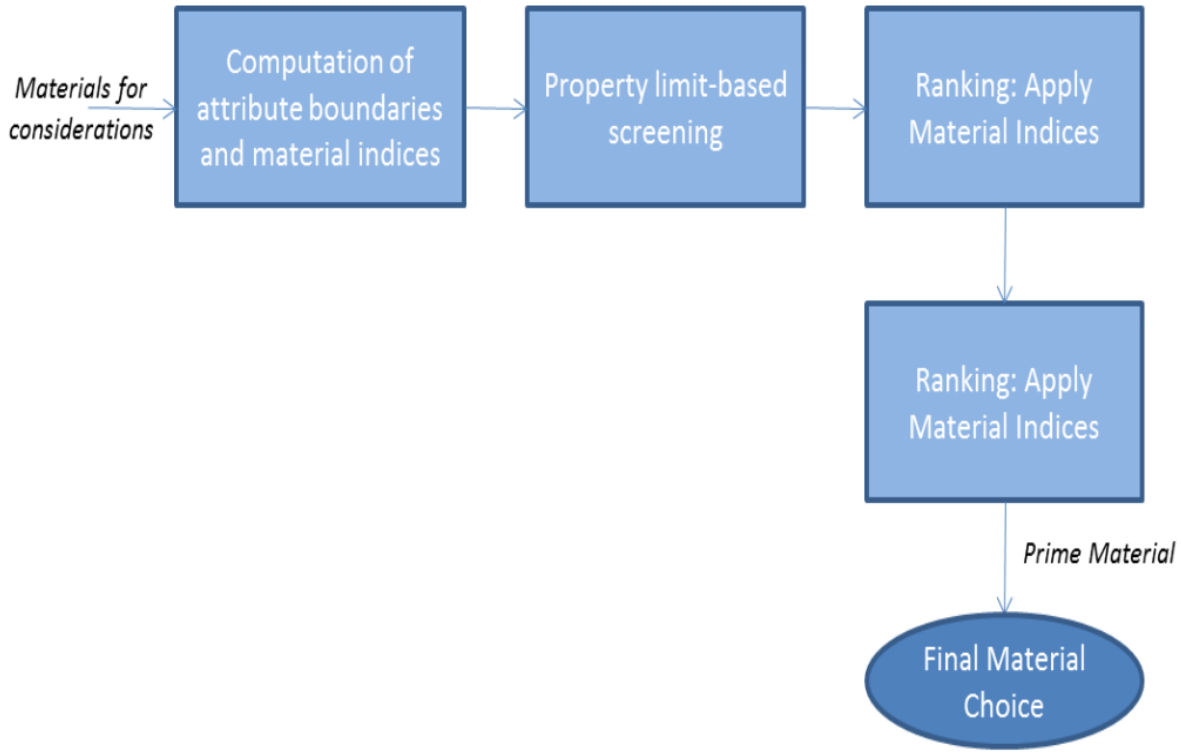

Figure 2: Ashby's Appraoch for material selection

3. RESULTS AND DISCUSSION

Using the Ashby's approach for selecting appropriate oxide and gate material, the initial procedure involves generating graphical representations of diverse material indices. Subsequently, it is necessary to impose limitations in order to determine feasible groupings of dielectric materials. The plot depicted in Figure. 3 illustrates the correlation between the permittivity of free space (ε_0) and the band-gap (E_g) of various high-κ dielectric oxide materials. It is evident that Si3N4, Al2O3, HfSiO2, Lu2O3, and La2Zr2O7 fail to satisfy the necessary criteria, as they necessitate an E_g of over 5 eV and a ε_0 of over 15. The materials that meet the specified criteria are displayed within the shaded rectangle.

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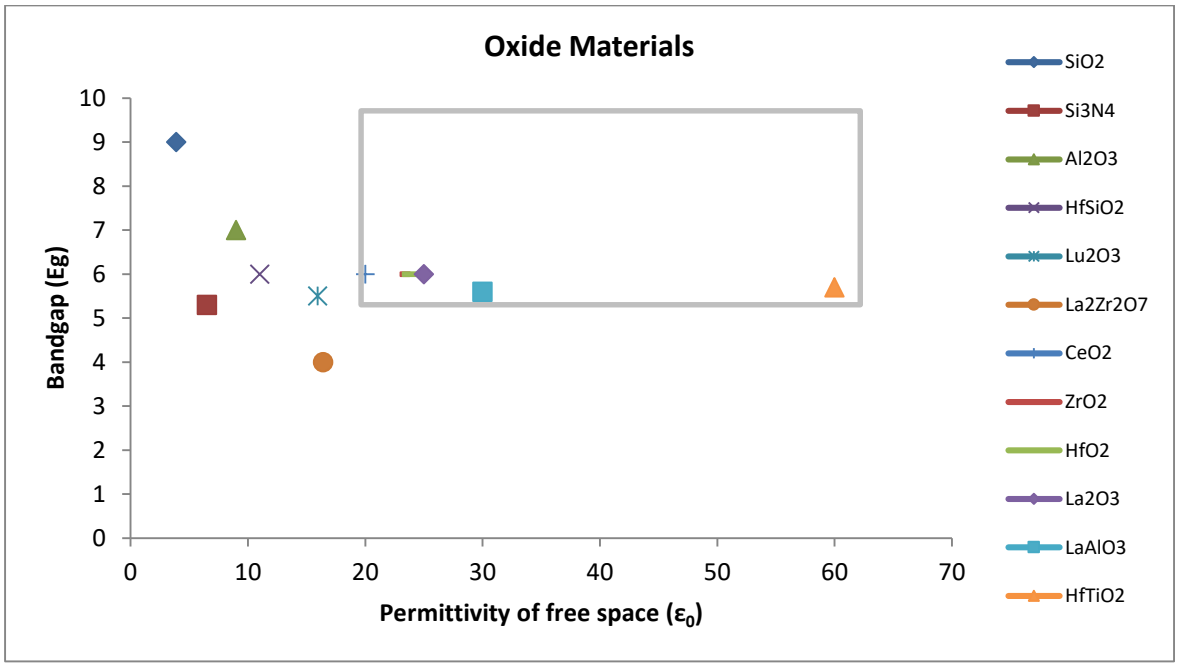

Figure 3: Dielectric HK material indices.

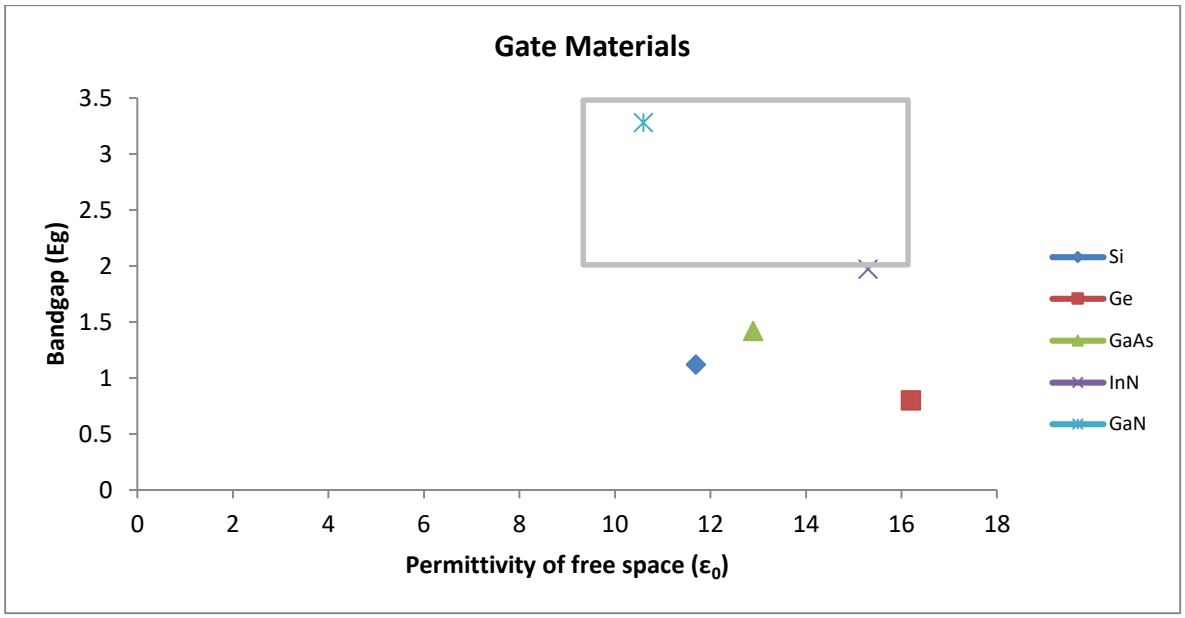

Figure 4: Dielectric MG material indices.

The plot depicted in Fig. 4 illustrates the relationship between the permittivity of free space and band-gap, specifically in regards to the various high-κ dielectric metal gate materials. It is evident that the materials Si, Ge, and GaAs do not meet the prescribed criteria of requiring an Eg greater than 2 eV and a ε0 greater than 10. Consequently, these materials are excluded from consideration as gate dielectrics. The shaded rectangle depicted in

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Figure. 4 encompasses all materials that meet the specified criteria. It is clear from Figure. 3 that the prime dielectric oxide material is HfTiO2 followed by LaAlO3, La2O3, HfO2, ZrO2 and CeO2. In a similar fashion the prime gate metal was found to be GaN followed by InN.

Table 3: Comparison of HK-MG materials interms of bandgap energy

Parameter	High-k (HK)Dielectric Oxide Materials									
	SiO2	Si3N4	Al2O3	HfSiO2	Lu2O3	CeO2	ZrO2	Hf02	LaAlO3	HfTiO2
E_g (eV) for Si as MG	0.78	0.72	0.689	0.669	0.65	0.641	0.63	0.63	0.631	0.613
E_g (eV) for Ge as MG	0.329	0.229	0.168	0.155	0.121	0.109	0.101	0.097	0.089	0.080
E_g (eV) for GaAs as MG	1.077	1.009	0.97	0.948	0.916	0.9	0.892	0.89	0.888	0.879
E_g (eV) for InN as MG	1.9	1.917	1.922	1.923	1.925	1.926	1.927	1.927	1.928	1.932
E_g (eV) for GaN as MG	1.708	1.46	1.351	1.296	1.222	1.19	1.173	1.169	1.203	1.148

Furthermore the Ashby's theoretical approach is supported by simulation of FinFET using variety of high-k dielectric oxide materials alongside various metal gates mentioned in section-2 to validate the material selection process. As seen from Table-3 it is evident that when compared to traditional Silicon (Si) as metal gate, the bandgap (Eg) is significantly less in case of Germanium (Ge) as metal gate which moreover decreases with an increase in k value. Similarly it is evident that when compared to traditional Silicon (Si) as metal gate, the bandgap (Eg) is notably more in case of GaAs and GaN as metal gate which experiences a decrease in Eg with an increase in k value. On the other hand it is noted from the simulation results that when compared to traditional Silicon (Si) as metal gate, the bandgap (Eg) is notably more in case of InN as metal gate which experiences an increase in Eg with an increase in k value.

At the outset, it can be observed that in the case of semiconductor materials, the electrons are primarily situated in the valence band, while the conduction band remains unoccupied. The disparity in energy levels between the aforementioned bands is referred to as the energy bandgap (Eg), which is contingent upon temperature. As the temperature of the semiconductor material increases, the thermal energy of the electrons within it also increases. Consequently, a reduced amount of energy is necessary to disrupt this bond. The decrease in Bond energy results in a corresponding decrease in the band gap. The temperature-dependent behavior of a semiconductor is such that its band gap diminishes as the temperature rises [17]–[19].

Compound semiconductors such as GaAs, InN and GaN are utilized in various applications. The group III-V semiconductors are classified as elements possessing three or five valence electrons. The elements boron, aluminum, gallium, indium, and thallium belong to Group III. Elements such as nitrogen, phosphorus, arsenic, antimony, and bismuth belong to Group V. The amalgamation of a group III constituent with a Group V constituent, results in the formation of a covalent ties comprising eight electrons, which leads to the creation of a distinct semiconductor.

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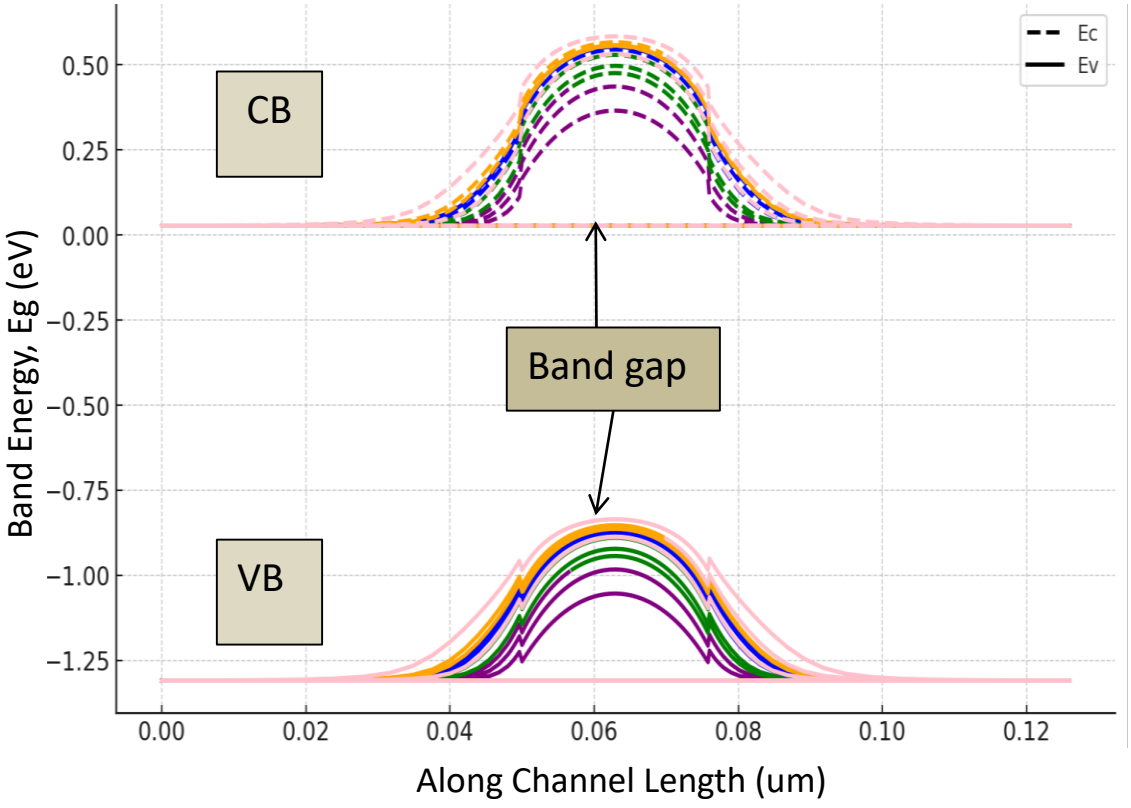
The following Figure 5 shows the energy band diagram for GaN along with Electric field distribution, current density distribution and surface potential for various high-k dielectric oxide materials. The broader density distribution of charge density and electric field is evident that the GaN pose to be a best candidate with high power density, higher mobility and less temperature dependent when compared to its counter parts. One example of a less dense substance is warm water, which occupies a greater volume relative to its mass. In contrast, it can be stated that cold water exhibits a lower density and occupies a comparatively smaller volume. Likewise, it can be inferred that a substance possessing higher density demonstrates a diminished melting point, while a substance with a lower density exhibits an elevated melting point. The analogy presented demonstrates that GaN in conjunction with HK, specifically HfTiO2, displays superior charge density and electric field density relative to other materials, making it an optimal choice for applications that are dependent on temperature. Also Upon examination of Figure 5(b), it can be observed that the electric field pattern exhibits radial outward direction from a positively charged point and inward direction from a negatively charged point signifying a strong electric field along the channel length. The negative potential observed in Figure 5(c) indicates that the Coulomb at a specific reference point along the channel length possesses lower potential energy. This indicates that the force of attraction between atoms in the case of GaN is attractive.



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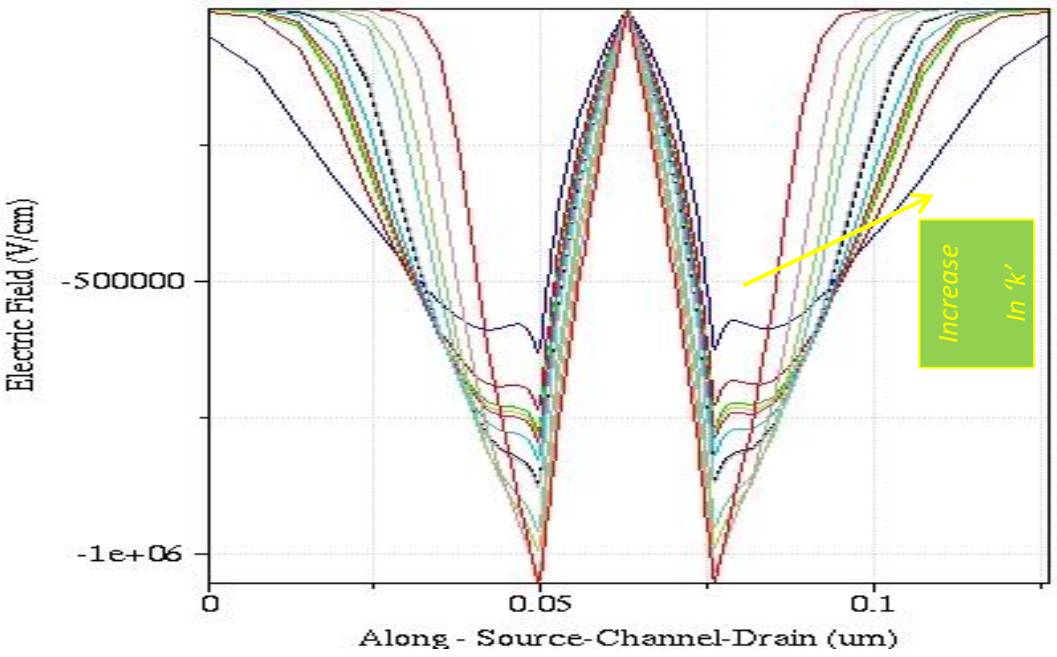

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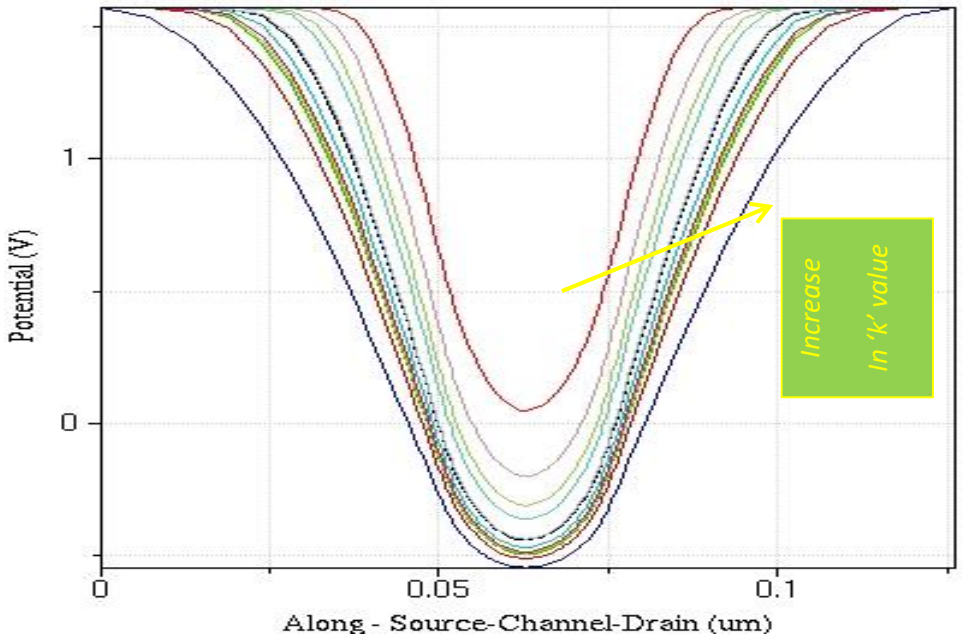

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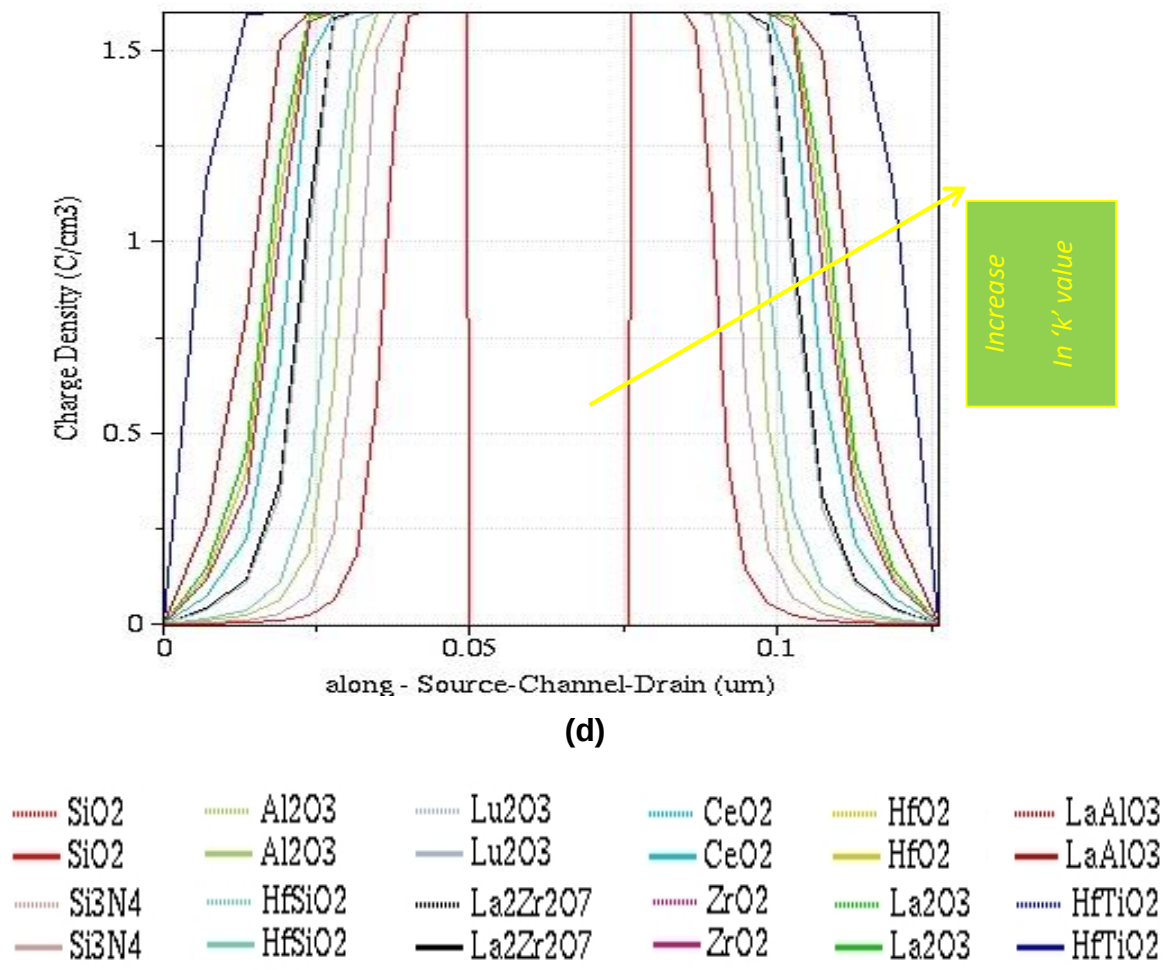

Figure. 5: (a) Energy Band diagram, (b) Electric Field Density, (c) Surface Potential and (d) Charge Density Distribution for MG as GaN using HK materials

4. CONCLUSION

The performance of multi-gate MOSFET devices has improved over single gate MOSFET devices suitable for applications in severe environments. The current driving capacity of such transistors grows as the number of gates increases. Utilization of FinFET with HK-MG increases gate control over the channel area. It also improves drain current and minimizes leakage current while maintaining short channel effects to a minimum. This study provides an overview of a variety of High-kdielectric oxide (HK) materials along with Metal Gates (MG) interms of energy band-gap, electric field distribution, charge density and surface potential. Semiconductors exhibiting superior electron mobility in comparison to silicon are deemed more advantageous in high frequency applications. The high power density of GaN, which refers to its capacity to dissipate heat from a compact component, is a remarkable feature that is complemented by its significantly high mobility. The conventional planar MOSFET device (2D) became the bottleneck of the rising demand

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for Systems on Chip (SoC) due to the continual progress in VLSI designs and architectures, as well as the quest of faster speed and ultra-low power electronics processors. Due to ongoing developments in VLSI designs and architectures, as well as the search for higher speed and ultra-low power electronic processors, the traditional planar MOSFET device (2D) has become the bottleneck of the expanding demand for Systems on Chip (SoC). This is due to the fact that VLSI designs and architectures continue to advance. Multiple gate architectures such as GAAFET, Multi-Bridge-Channel (MBC) FET, and Forksheet FETs are required to meet the growing need for improved device leakage control.

Conflict of Interest Statement: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest. No other potential conflicts of interest relevant to this article were reported by the authors.

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