Tianjin Daxue Xuebao (Ziran Kexue yu Gongcheng Jishu Ban)/
Journal of Tianjin University Science and Technology
ISSN (Online): 0493-2137
E-Publication: Online Open Access
Vol: 55 Issue: 07:2022
DOI 10.17605/OSF.IO/F375Z

ERROR CONTROLLING TECHNIQUES IN FLASH MEMORIES: A REVIEW TO MANY LOGICAL APPROACHES

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ABSTRACT:

Due to its high overwriting concept, flash memories play a critical role in the VLSI sector for data storage. However, because of the parasitic capacitance that exists between the storage cells, errors in decoding the memory circuits occur. Many error control coding techniques have been created in information coding to repair errors, such as RS decoding, BCH decoding, and LDPC decoding, which are all utilised as error control coding in NAND flash storage. Controlling different voltage levels shows the difference between soft and hard decisions in error control strategies. The best result on various output leads is obtained by fragmenting NAND Flash into pages with a threshold and applying various techniques such as paired pages and parallel pipelined techniques. In this survey, we analyse the results of diverse approaches, strategies, tools, and techniques employed to decode NAND flash memories with various error control encodings.

Keyword: NAND flash, LDPC, BCH

I. INTRODUCTION TO NAND

NAND flash memory is a semi flash resource which can store data even after the system is removed off. The majority of current sources, such as cameras and mobile phones, use NAND flash memory storage. Dr. Fiyio Masuoka of Toshiba Corporation invented the first flash memory in 1984. NAND flash memory has a faster processing time, is reasonably inexpensive, and has authority longevity. NAND memory can be scalable on both an univariate cell (SLC) and a multi-level cell (MLC). NAND flash memory have a fast access time, a relatively inexpensive, and a commission based endurance. Single Level Cell (SLC) and Multi-Level Cell (MLC) NAND memory can be scaled (MLC)[1]. One of the major scaling issues is that the number of electrons kept in the control gate decreases significantly with each process generation. This has implications for the detection of the stored data value as well as data retention. This phenomenon, when paired with inter-cell interference Signal processing procedures can be disrupted as a result of parasitic capacitance. Each NAND string in the cell interface has a positive voltage contact with another sequence signal applied that is linked by word lines (WLs). Every NAND Flash cell forms a memory array in which it can read, write, and erase additional circuits [2]. Because the memory cells are arranged in a matrix, every cell along the word line is biased at the same voltage, even if it is not intended to be programmed. They're dispersed, to put it that way.

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II. INTRODUCTION TO ERROR CONTROL CODING

Bit-errors in memory are corrected using Error Correction methods. To detect and repair errors, Check-bits are used to introduce redundancy in error correction[3]. When k bits of unreliability are added to an m-bit message, the result is a m+k (=n) bit wide code word. There are a total of 2N potential combinations out of such a total of 2N different permutations, Most would be acceptable code terms(i.e. zero errors) and the part would be pro words (Considering a fault, for example). “When a non-code word is found, "error detection" occurs. In order for "Debugging" to occur, It must be recognized how many of the ones that follow code word The inaccuracy is represented by bits. The code word bits are generated by an Error Correction Coding encoder by including binary representation into the digital information. This information will be restored in memory. An Error Correction Coding decoder is used to examine and after the data has been read out, discover mistakes [5]. To detect errors, the decoder employs The parity-check matrix, user bits, and parity bits (H-Matrix).

A. PARITY AND HAMMING CODES

Hamming and Parity Codes The parity code is the most basic error detection code. A To make the parity of the code word bits even, a bit is added to the message bits (or odd)[5]. Despite its simple design, a parity code can identify a single inaccuracy. When two bits shift, the parity remains constant, and the errors are undetected. Hamming codes are capable of fixing single-bit faults as well as detecting Errors impacting two bits (SECDED). Correction of a single error The Hamming code utilises an H-Matrix with no repeating columns and almost no all-zero entries (SEC). A single bit error detection with alteration system The H-Matrix in Hamming code (SEC-DED) is similar, but with additional parity bits. To rectify multi-bit errors, Reed Solomon and BCH codes are utilised.

B. CODES FOR BOSE, CHAUDHURI, AND HOCQUENGHEM (BCH)

This is a type of cyclic error handling code that can be used to repair complicate in NAND Flash storage[2]. A valid code word's cyclical shifting yields in some other suitable decoder, which is unique to code words. There are two primary phases involved in the generation of BCH codes: Step1: Making a generating polynomial G (x), Step2: Encoding the information. A message of k bit samples is encoded into an BCH coding of binary form word using the generating polynomial.

C. REED-SOLOMON CODES

Reed-Solomon codes are a subclass of BCH codes and are a sort of linear binary sequence. Reed-Solomon codes (n-k)mt and BCH codes: (n-k)mt 2t=(n-k). Thus, for a k-bit message, 2t check bits are added to produce an n-bit Reed-Solomon code word[18]. This type of code can repair t-bit mistakes. Reed-Solomon codes are optimal because the lowest distance for an RS code is 2t+1 = (n-k+1), and the 17 shortest range (n-k-1) is the high feasible number for a linear code of block length n. Reed-Solomon codes can also be transformed to a non-binary format by using a symbol-based encoding. The benefit of symbol-based encoding is that it may be used to fix burst errors. Every character

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is specified as being m-bits long. This is due to the fact that If an inaccuracy is found in a pattern, the overall pattern must be rectified. As a result, for burst mistakes, this is an effective correction strategy.

D. LOW DENSITY PARITY CODES (LDPC)

Low density parity codes are a error-correcting linear block codes. These codes have scarce H-Matrices sets them apart[13]. They have a very high performance rate for big block lengths, This is accurate to the Shannon Capacity, as a result, they are widely used for error correcting algorithms. Because of its capacity to handle both hard-bits and soft-bits datum, LDPC codes be used to generate convolution codes from block codes[16]. As a result, it performs well when There is both soft-bit and hard-bit information present.

E. TANNER GRAPH

There are three techniques to define a linear block code: 1)Generator Matrix. 2)Tanner Graph is a graphical representation. Tanner Graphs are frequently used to represent LDPC codes[17]. Tanner Graph is a bipartite linear representation with two deviating denomination of nodes.: 1)Bit Nodes —Nodes that represent the code word bits. 2)Check Nodes — Nodes that denotes the parity check mathematical statements. If and only if a given code word connects important check mathematical statemets, a line reflects the correlation between bit node and check node. Tanner Graphs are widely used in LDPC decoding algorithms. Messages are iteratively exchanged along the edges of the network between the bit nodes and the check nodes. The bit nodes send messages to the check nodes first, disseminating the bit nodes values. Following the receipt of data inputs from all of its associated bit nodes, each checking node uses its check mathematical statement to calculate appropriate readings by each bit nodes and distributes the indicated received data to the bit nodes. If necessary, for every bit nodes adjusts its very own datum and transfuses the cue back to the check nodes. This operation do repeated repetitious, with memorandum being transmitted extremity and onward betwixt bit nodule and check nodule until all parity check mathematical statements are fulfilled [15].

III. ERROR CONTROL CODING IN FLASH MEMORIES

Hard-bits and soft-bits data information can be obtained from flash memory, which can then be transferred to the error circuit for decoding for detection and correction of faults[1] . With the combined objective of enabling to process both hard and soft data information, the performance of error control codes is fairly near to theoretical bounds, such as the Shannon Capacity Limit.

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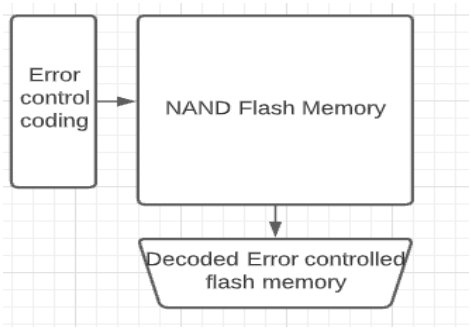

Fig: Implementation of ECC in Flash Memories

Correction of miscue in NAND flash memory chips is accomplished through the use of an ECC encoder and decoder. The block diagram above depicts how error control coding is implemented in flash memory using neural network method. In this method VLSI with AI concept can be used for correcting the flash memory using error control technique. Error control coding in NAND memory is influenced by three key factors.

A. Scaling

As the cell size shrinks in shrinking technology nodes, There are lesser atoms captured inside the floating Gate of NAND flash memories. This raises unpredictability of the programming to a certain voltage threshold.

B. Cycles of Program/Erase [P/E]

The number of P/E cycles that NAND Flash memories may withstand before failing is restricted. The more frequently P/E cycling occurs, the worse the cell deteriorates, resulting in higher in trifle.P/E cycles are typically 100,000 times for Single Level Cell of NAND flash memories also roughly 10,000 times for Multi Level Cell NAND flash memories.

C. Multi-Level-Cells(MLC) Technology

The statistics of bits-per-cell upsurge, so complexity of the system increases and this reduces the difference which occurs in nearby Voltage Threshold distribution. As a result, there is a greater chance that a bit will end up in the incorrect Voltage Threshold window, resulting in a bit mistake. As a result, bit mistakes are more likely in systems with more bits-per-cell. As a result, MLC memories contain a higher number of bit mistakes, necessitating the adoption of stronger ECC methods. Because of the 8-state voltage distribution, the amount of bit-errors in TLC (Triple-Level-Cell) technology is even larger. This can be reduced by improving optimization algorithms to produce narrower Voltage Threshold dispersion or by implementing robust ECC systems to correct the associated bit errors.

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NOR flash memory consumes more power because it does not require error correction[21], whereas NAND is designed by n MOS transistors, which require one bit line contract in each string of the matrix, this may lead to error when connected with parasitic capacitance, which is placed in between storage cells [1], As a result, error detection and correction is very essential for NAND flash Memory chips. The literature study mentions numerous ways for correcting NAND flash memories and various algorithms is implemented to decode the errors and faults for the same.

IV. LITERATURE REVIEW

Extensive research on both error controlling technique and NAND flash memory has been conducted over the last several decades. Many algorithms and approaches have been developed to create error control coding for NAND flash memory using various methodologies and criteria.

Jonghong Kim, Wonyong Sung [1] has suggested a VLSI approach for implementing a pace of 0.96 (68254, 65536) Parity of Euclidean Graph-Low Density Check code for Flash Memory data soft-decision error correction using a five-stage parallelizing eight-way deep networks for signal integrity, To reduce complexity, It also includes several chip area control strategies like word-length refinement, compaction of sign variable outputs, and approximation of the second minimum using an APP-based algorithm with conditional node updating. Performance is measured based on pipelining concept but not much compare with other coding technique.

Sung gun Cho and et al [2] Iterative hard decision decoding (IHDD), a decoding technique based on iterative reliability, was introduced for NAND flash storage.The author attempted to create a powerful error correction and the results of a significant rate defect monitoring system for storage devices were compared to the results of other error control systems, yielding good trade-offs between performance and complexity. In this performance measured based on reliability of the flash memory.

Sangha Lee and et al [3] presented a NAND flash memory paired page reading technique in which each wordline is made up of two logical pages, the MSB and LSB pages. The data from these two logical pages is used to create symbols that are employed in the programming of memory cells for NAND flash memory using a joint decoding and signal processing approach. When the raw error rate is dependent on voltage level, this provides a significant gain in error correcting capability. This also ensures that both qualitative and quantitative measurements are maintained in paired page.

Weidong and et al [4] worked on Optimized Computation Cycle Elimination (OCCE), development of RS, QC LDPC codes for fast coding with short cycle reduction, and concatenation of both codes, The observed factor is two separate error control codes that are concatenated and analyzed the coding for NAND flash memory in short cycle, and

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the results are compared in QC LDPC. This paper achieves higher performance while reducing decoding complexity using two decoding technique
Lita Yang and et al [5] in this article, The author investigated the idea of a convolution neural network processor using CIFAR binaryNet and computed on ConvNet implementation to achieve bit error tolerance and determine the efficiency in SRAM voltage scaling, resulting in memory energy savings in multilayer networks; this analysis is compared to other networks and demonstrated in bit error requirement.

Arul K Subbiah, Prof Tokunbo Ogunfunmi [6] In this section, we can see error correction utilising BCH codes for flash memories using GPU, as well as its memory efficiency. C programme for compute unified device architecture (CUDA), This paper considers extended Euclidean algorithm, extended BCH decoder for higher - level bits error detection, convolutional BCH encoder, and z domains Mode BCH encoding. We get a clear picture about using cov BCH to make error correction to NAND flash memory and this extends its novelty with machine learning concept with GPU and LUT table.

M Kim , M Liu and et al[7]In this design, scholar investigate the hardware and software design for 3D NAND flash based CNN with physical implementation using back pattern dependency cell current can be measured, we can vision deeply that 3D NAND flash eNAND cell is demonstrated using DNN approach for standard logic cells. There is no error control coding approach occurred in this and hence we can make use of this gap for our research

Cheng Wang and et al [8] The author employed the approach Non binary Majority Logic parallel scheme for check nodes in flash memory, author noticed that conventional majority logic decoding we can enhance FER performance and speed, but the author can be notice that method can be extended to TLC NAND flash memory. By making it to more parallel, it improve throughput and achieve more performance in FER Liyan Qiao and et al [9] suggested a Joint Decoding Strategy of Non Binary LDPC Codes Based on Retention Error Characteristics for MLC NAND Flash Memories, proposed the work with approaches Joint decoding strategy, belief propagation algorithms, Non Binary Low Density Parity Check decoder algorithm , FFT of posterior probability, Analysis of retention Error Characteristics in NAND Flash memories using Soft Information in Non Binary LDPC, Using FFT posterior probability block of the flash memory is handled.

Toshiki and et al [10] in this paper the writer mentioned about use of neural network in low density parity check codes for both 3D and 2D NAND flash memory with the concept of charge type and floating gates scenario . they mentioned about the static information with worline, adjacent cell data and read offset level. Artificial neural network convolution method is adopted for error control coding which impact on coupling noise which maintain good retention data rate

Md Bavandpour and et al[11] a case study of 3D NAND flash memory using time domain VMM approach and compare the case with word line, bit line, load capacitance and other

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embedded is done. we clearly observe that no ECC concept deal with this paper, so we can make this a study literature gap and can further implement this for ECC decoding technique in the as study of Word line and bit select line
Bradley comar [12] LDPC codes is automated using CNN and Analysis the result for LUT with testing for CNN Markov chain algorithm is implemented with probability distribution for correct codes, this method helps in linearly rate and comparing the performance in linear rate, but no application is found, so this can be consider as research gap, so we can use this analysis of LDPC with CNN at the LUT with RS LDPC technique too. Using NAND cell we can fill the gap

The following table briefly explains about various technique, methods, algorithms and its respective outcomes.

Sl no	Authors	Title of the Paper	Methods/Algorithms	Outcome/Result
1	Jonghong Kim, Wonyang sung	Soft-decision decoding for reduced error detection and correction in MLC Flash memory	Memory signalling processing, forward Error correction, accuracy factor affecting on iteration count, and soft decision error correction approach	Error correcting for NAND Flash can be accomplished using LDPC's soft decision error correction. By adjusting the page (column) matrix, it is possible to read multibit data for word line voltage.
2	Sung gun Cho and et al	Shuffled Block Wise BCH Codes for Nonvolatile Memory chips	Iterative hard decision decoding technique (IHDD), Iterative reliability-based decoding technique (IRBD).	In this paper, We have discovered block-wise concatenation BCH for NAND flash
3	Manisha G Waje, Dr P K Dakhole	Development and performance evaluation of a single-layered reversed parity generating and parity checkers based on the Nanoscale Cell Lattice framework.	Error detection through the N-1 bit coding approach and the Optimized Feynman gate	The XOR gate's simulation parameters are compared with cell count, area, crossover, and latency using the Optimized Feynman gate.
4	Mingliang Zhang and et al	Turbo Encoder Simulation model in Nanoscale Automata	Pipelining in two stages, R C encoder with single and multiple feedback	QCA is used to construct a turbo encoder with single and multiple feedback.
5	Sangha Lee and et al	Vlsi Memory Chips Matched Page Accessing Technique	Each word line is made up dividing into two logic pages, the MSB and LSB The information from these	In this work two pages are paired with single voltage line sensor and hence it form paired page. Low latency is achieved

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			two logical pages is used to generate symbols that are used in memory cell programming.	
6	Liyan Qiao and et al	A Detection Initiative for Non-Binary LDPC Codes Based on Retention Error Patterns for MLC NAND Flash Memories	Joint decoding strategy, life prediction method, NB LDPC decoder technique, posterior probability FFT	Retention Error Analysis Characteristics in NAND Flash memories are handled using Soft Information in NB LDPC, and the posterior probability block of the flash memory is handled using FFT.
7	Prerana Dhanokar, Monica Kalbande	Design of LDPC Decoder Using Algorithm for Passing Messages	Sum Genetic algorithm, product algorithm, Min Sum Algorithm.	The basic block from the simulunik library was used to create the check node and variable node. Simulink HDL codes were used to generate HDL codes for check nodes and variable nodes.
8	Wie Lin and et al	Advance Signal Processor 3X Longevity Advancement for 3D Flash Memory	Signal Processing Algorithm, Noise Cancellation Method to Reduce CTCI Using an n-1 times read operation, divide the neighbouring data into n separate portions, and read data on a selected word line. with a n different read voltage, and aggregate the data from the n times read operation.	Signal processing algorithms are used to reduce aspect ratio and cancel noise across NAND flash memories.
9	Arul K Subbiah, Prof Tokunbo Ogunfunmi	Error Control Tactic for Flash Memories that is Memory Economical Leveraging Graphics	C software for computing unified device architecture (CUDA), Extended Euclidean method, extended BCH higher order bit error detection codec. convolutional BCH encoding, as well as a multimode BCH codec in the z domains	This work provides a clear picture of how we can fix errors in NAND flash memory using cov BCH. And to this extent, it is novel with machine learning concepts such as GPU and LUT tables.

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10	Wenjie and et al	Dynamic Benchmark Form LDPC Encoder NAND Flash Memory Voltage Algorithm Based	Monte Carlo simulation for threshold voltage analysis, belief propagation (BP) algorithm, expectation maximisation (EM) Detection technique based on dynamic reference voltage APPROACH: Incremental step pulse programming (ISSP), channel model and LLR calulation, and cell-to-cell interference	Estimation maximisation (EM) can be used to estimate the mean and variance and obtain good retention noise, while LLR can be used to improve the channel.
11	Jieun and et al	A New Symbol Freaking Automated system for Non-Binary LDPC Codes and Its Deployment to NAND Flash Memories	Algorithm for Symbol Flipping Decoding (SFD). The DRB-SFD technique is also The q ary sum product algorithm is also known as the q ary sum product algorithm. A unique SFD algorithm is decision symbol reliability based SFD.	For LDPC NAND flash memory, the Symbol Flipping Algorithm is employed. We learn through the implementation of this work that there is an improvement in the error rate performance for Hard decisions..
12	Toshiki and et al	Adaptive Artificial Neural Network(A2N2) coupled LDPC ECC as universal solution for 3D and 2 D, charge trap and floating gate NAND flash Memories	ANN with LDPC algorithm	Five cases of ANN LDPC with input parameter V_{th} state, page type, wordline number, adjacent cell data and read offset level. by the same tool..
13	Cheng Wang and et al	Adaptive 2D scheduling based Non binary Majority logic Decoding for NAND Flash Memory	Non Binary Majority logic (NBMLGP), parallel scheme has been added for CN"s and executed ATS, correcting ATS algorithm, parallel algorithm	Improved error performance by pursue superior error correcting capability and early correcting (EC). Simplified message passing process of ATS

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14	M Kim , M Liu and et al	A 3D NAND flash ready 8-bit convolution Neural network core demonstrated in a standard logic process	DNN with Multiple computation layers, leNet 5 CNN with MNIST, compute in memory(CIM), computation, bit column state(BiCs), eNAND Cell	using Neural network a general framework is design eNAND standard logic cell using leNET CNN
15	Md Bavandpour and et al	Mixed signal vector by matrix multiplier circuit based on 3D nand flash memories for neurocomputing	Time domain 3D VMM, Embedded approach in tool, case study with DTC, 3D FM, CAP, NB, TDC, WL`, BSL`	case study of 3D NAND flash memory using time domain VMM approach and compare the case with word line, bit line, load capacitance and other embedded
16	Weidong and et al	RS LDPC conjunction source code for NAND flash memory: Design and short flow optimization	Optimized Computation cycle elimination (OCCE), Construction of RS, QC LDPC codes for fast coding with reduction of short cycles, concatenated both the codes	Two different error control codes are concatenated and analysed the coding for NAND flash memory in short cycle, this result is compared in QC LDPC
17	Cristian Zambelli and et al	The First Case of Temporary Read Error in Tri Layer Cell 3D NAND Flash Memories Trying to leave an Active State	Layer Normalization by boxplot test case, TCAD simulation tool, Cumulative distribution function(CDF)	We can view that designer developed 3D NAND Flash by fail bit count statistic concept while occur in idle phase of first read operation on block while latering threshold voltage
18	Bradley comar	Analysis of CNN based scheme for LDPC code classification using LUT based algorithm	DL Network, ReLu train Network, smart LUT training and LUT testing Algorithm:1) Probability distribution of final state in pure birth Markov chain, Calculate probability of smart LUT method choosing the current codes	LDPC codes is automated using CNN and Analysis the result for LUT with testing for CNN Markov chain algorithm is implemented, this method helps in linearly rate
19	Lita Yang and et al	CIFAR (Canadian Institute For Advanced Research)-10 Binarized Convolutional Internet	CIFAR 10 binary net, binarized neural network(BinaryNet)	we can observe the bit error tolerence in SRAM, SRAM volt sliding efficacy in a 9 lane Canadian Institute For Advanced

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		backbone Processor Frame Error Resilience		Research(CIFAR) 10 binarized deep convolutional neural network, this is implemented in 28nm processor and achieved memory saving
20	Eliya Nachmani and et al	Computational Intelligence Method for Improving Polynomial Code Interpreting	Deep Learning Method, RNN Architecture, Neural Belief Propagation decoder, Neural Min sum Decoding, RNN Decoding, Modified random redundant iterative algorithm(mRRD), Neural BP Algorithm	LDPC is decoded using different value of N, Deep Learning method of improves the ECC

V. CONCLUSION

At the first stage of the research survey, we come to know that NAND flash memories need error correction[1] and we analyse many methods proposed in VLSI for correcting the error, we identifies that paging method is one among where column matrix is adjusted . We also learn that the paired page[5] concept may be employed for reading matrix but they did not implemented parallel page reading method which can optimized computation cycle elimination and used for quickly computing error codes in NAND Flash storage. Neural network section of the survey illustrates how Machine Learning and neural network techniques can be applied for error control coding for SRAM[19] and the operation of convolution BCH codes employing GPU and LUT but this method is not implemented for NAND flash memories with LDPC codes where we may obtain much better result that other techniques which mentioned so far . ANN method can be used for LDPC codes [18] but it is not been implemented for any kind of flash memories. So, based on all of these survey techniques, we can conclude that employing neural networks improves the decoding efficiency of NAND flash memory for paired paging which is not yet implemented in those research, and hence we can come with the conclusion that using ANN approach for LUT with the combination of error controlling decoding techniques bit error is reduced by multi correction analysis, and efficiency can be boosted. Using the convolution neural network decoding technique much better result can be obtain.

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