# BINARY HYBRID 31-LEVEL MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

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#### Abstract:

A binary hybrid 31-level multi-level inverter is proposed in this paper for medium voltage applications, and compared with a conventional cascaded H-bridge inverter. The main drawback of conventional topology is a large number of power supplies and semiconductors required to generate these multistep voltage waveforms. Due to the hybrid structure inverter, 31 levels can be manufactured with the fewest number of components, as only 12 switches were used. As the number of output voltage levels increases, the proposed architecture reduces the number of IGBTs and gate driver circuits significantly. The proposed inverter can generate high-quality output voltage close to the sine wave. The circuit of the hybrid inverter and cascaded H-bridge inverter was simulated using the MATLAB program. A fast Fourier transform analysis of the output voltage waveforms was performed, which resulted in a total harmonic distortion value of 3.60% in the hybrid inverter while the total harmonic distortion value was in the bridging modulator. 3.74%.

**Keywords**: Multilevel-Inverter (MLI), Cascaded H-Bridge multilevel inverter (CHB-MLI), Total harmonic distortion (THD), Hybrid Multilevel inverter (HMLI).

#### 1. INTRODUCTION:

In high-power applications, multilevel inverters (MLI) are becoming more popular than two-level inverters [1] [2]. Conventional two-level inverters require a high switching frequency to produce a quality output voltage waveform, whereas MLI can produce more power by combining several power switches with multiple low voltage dc sources [3][4]. All switches in multilevel inverters are connected in series, allowing them to operate at higher voltage levels [5]. MLI has several advantages, including high voltage capability, low switching losses, low DV/DT, less THD, and lower electromagnetic compatibility [6][7].

The neutral point converter, flying capacitor, and cascaded H-bridge multilevel inverter are the three main MLI configurations [8] [9]. CHMI has more benefits than the other two mentioned. CHMI Cascaded H-bridge multilevel inverters, as shown in the figure (1), have gotten a lot of attention because of their advantages like low component count which lacks flying capacitors and clamping diodes., reliability, and modularity [10]. To obtain a sinusoidal output voltage wave, multilevel inverters can increase the number of output voltage levels. It will, however, necessitate more components, increasing the complexity

and cost. To overcome the disadvantages listed above, a hybrid multilevel inverter derived from a cascaded H-bridge inverter is used [11] [12].

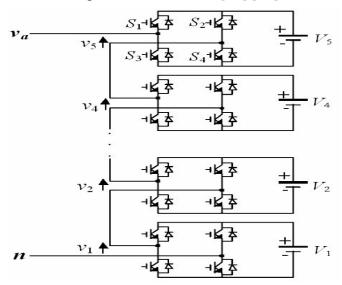


Figure (1): structure of cascaded H-Bridge

#### 2. MODULATION METHOD:

When it comes to multilevel voltage source converters, the first thing that comes to mind is the requirement for a large number of switches, which can result in a complex pulse-width modulation (PWM) switching scheme [13].

Modulation is the process of turning on and off the power electronic switches of an inverter in a specific sequence to achieve a nearly sinusoidal waveform [14]. Modulation techniques are classified based on the switching frequency, as shown in Figure.2.

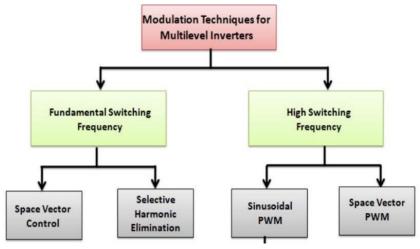


Figure (2): classification of Modulation Techniques

Fundamental switching frequency techniques require only one of two power semiconductor switch commutations per output voltage cycle [15][16]. In a Sinusoidal PWM technique, a single sine wave is compared to a triangular (carrier) wave to generate pulses for an inverter's switching operations. By using a larger number of carriers, a sine PWM technique has been extended to multi-level inverter modules [17]. As a result, it is simply known as multi-carrier pulse width modulation. Multi-carrier-PWM (MCPWM) is the most common and simple switching scheme for multilevel voltage source converters [18] [19]. For an n-level inverter, (n-1) carrier waves are required. Each carrier signal is continuously compared to the voltage reference as shown in Figure.3 [20]

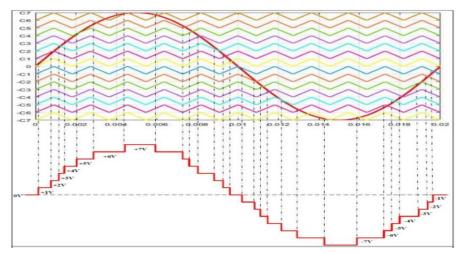


Figure (3): Generalized stepped waveform by using (MC-PWM)

Multicarrier-PWM technology can be divided into two parts: Level shift-PWM and Phase Shift-PWM LSPWM is again divided into three types [21] [22]. They are:

- 1. Phase Disposition-PWM (PD-PWM)
- 2. Phase Opposition Disposition-PWM (POD-PWM)
- 3. Alternate Phase Opposition Disposition-PWM (APOD-PWM).

This paper describes a Hybrid multilevel inverter that employs a binary dc input source and a minimum number of switching devices [24]. As a result, control is simplified and straightforward. In addition, MATLAB embedded function for constant voltage and constant frequency operation is written.

The conventional topology has four switches in an H-bridge unit, but the proposed topology has only two switches in an H-bridge unit [25]. As a result, the number of keys used will be halved leading to control being simplified, easy, and economic [26]. Switching losses are also significantly reduced. Figure 4 depicts a basic concept for generating output voltage levels where Vdc1=VDC, Vdc2= 2VDC, Vdc3= 4VDC, Vdc4=8VDC.

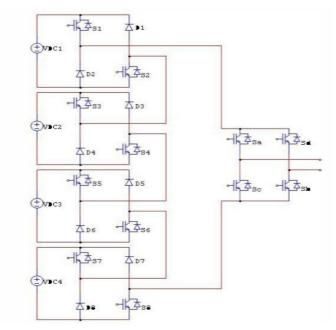


Figure (4): Proposed Hybrid topology for 31 levels

## **3- HYBRID MULTILEVEL INVERTER TOPOLOGY WITH THE FEWEST SWITCHES**

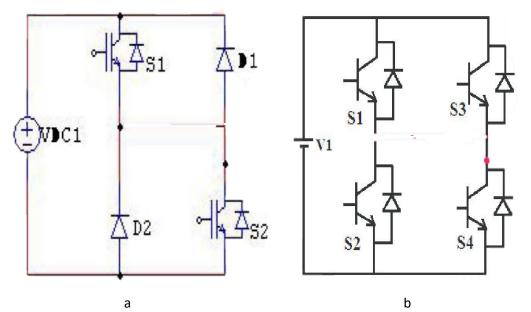


Figure (5): Basic unit of MLI. (a) Conventional cascaded H-bridge topology (b) Proposed Hybrid topology.

Figures 5(a) and 5(b) show the basic unit of a multilevel inverter in the conventional cascaded H-bridge and proposed hybrid topologies, respectively. The conventional cascaded H-bridge topology has four switches in an H-bridge unit, whereas the proposed

Hybrid topology has only two switches in an H-bridge unit. As a result, the number of switches is reduced by half, as are the gate driver circuits. As a result, control is simplified, easy, and cost-effective. Switching losses are also significantly reduced.

#### Table 1: conventional topology with switching patterns

S1&S2	S3&S4	Vo
1	0	+V <sub>DC</sub>
0	1	- Vdc

#### Table 2: conventional topology with switching patterns

S1&S2	Vo	
1	+V <sub>DC</sub>	
0	- Vdc	

Tables 1 and 2 show the switching scheme and output voltage for the conventional and proposed topologies, respectively. When (S1& S2) is turned on, the output voltage is +VDC, and when (S3 &S4) is turned on, the output voltage is -VDC. In the proposed topology, when (S1 &S2) is turned on, the output voltage is +VDC, and when they are turned off, the output voltage is -VDC, provided the diodes (DI&D2) are connected to a higher potential. As a result, the proposed topology allows for the distribution of DC voltage sources in a binary pattern.

The topology employs a binary dc input source. By using VDC, 2VDC, 4VDC, 8VDC it can synthesize 31 output levels: VDC, 2VDC......14VDC, 15VDC as shown in table 3.

<b>S</b> 8	S7	<b>S6</b>	S5	S4	S3	S2	S1	V
0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	1	1	1
0	1	0	1	1	1	0	1	2
0	1	0	1	1	1	1	1	3
0	1	1	1	0	1	0	1	4
0	1	1	1	0	1	1	1	5
0	1	1	1	1	1	0	1	6
1	1	0	1	0	1	0	0	7
1	1	0	1	0	1	0	1	8
1	1	0	1	0	1	1	1	9
1	1	0	1	1	1	0	1	10
1	1	0	1	1	1	1	1	11
1	1	1	1	0	1	0	1	12
1	1	1	1	0	1	1	1	13
1	1	1	1	1	1	0	1	14
1	1	1	1	1	1	1	1	15

#### Table3: Conventional Topology with Switching Patterns

#### Simulation results:

A 31-level inverter model in MATLAB/Simulink has been created the total harmonic distortion is used to evaluate the quality of the output voltage waveform (THD).

Figure 6 depicts the MATLAB/Simulink model of the proposed topology. Figures 7 and 8 show the simulation results for output voltage, and total harmonic distortion

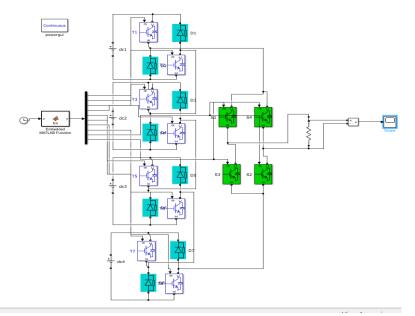


Figure (6): MATLAB/Simulink Model of Proposed Hybrid Multilevel Inverter

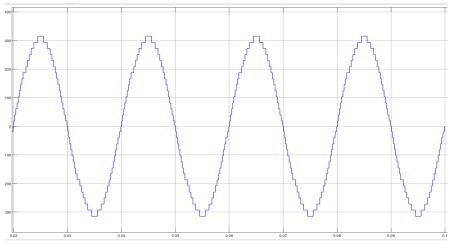


Figure (7): Output Voltage for 31 Levels

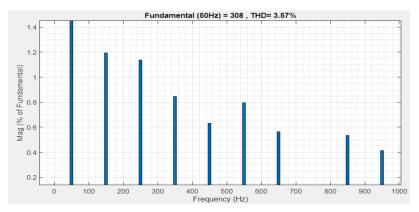


Figure (8): THD% of voltage waveform of 31 level in proposed Hybrid multilevel inverter

While the simulation results of the cascade H-bridge multi-level inverter to generate 31 levels using the multi-carrier pulse width modulation technique were as shown in the following figures:

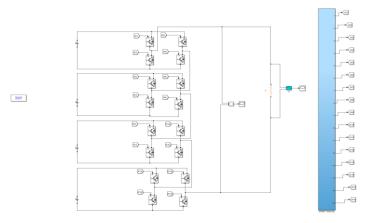
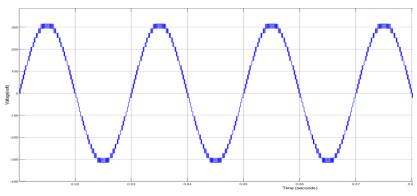


Figure (9): simulation model of 31 Level-Cascaded H-Bridge inverter





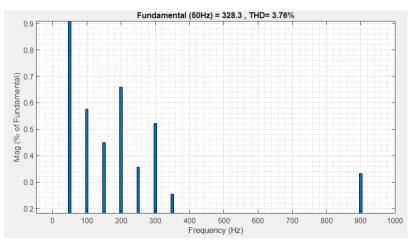


Figure (11): THD% of voltage waveform of 31 levels in proposed hybrid MLI

# Table (2): comparison between cascaded H-Bridge and Hybrid multilevel inverter to generate 31-level

Type of Typology	Number of switches	THD%
Hybrid MLI	12	3.60%
Cascaded H-bridge MLI	16	3.76%

### 4. CONCLUSION

For the multilevel converter, a new multilevel module (MLM) has been proposed. The proposed topology combines MLMs and full-bridge converters. The proposed Hybrid topology increases flexibility in design and the converter's capability to be optimized for various goals. Cascaded H-bridge topologies have been compared to the proposed Hybrid topology. It has been demonstrated that the proposed Hybrid topology provides 31 output voltage levels using 12 IGBTs. While, the Cascaded H-Bridge topology generates 31 voltage levels with 16 IGBTs. The proposed topology may be a good solution for applications that require high power quality or a large number of dc voltage sources. The proposed topology's operation and performance have been validated using computer simulation. Analyses and simulations demonstrated the proposed system's superiority.

#### Reference:

- R.Bensraj, S. P. Natarajan and V. Padmathilagam, "Multi-carrier trapezoidal PWM strategies based on control freedom degree for msmi," RPN Journal of Engineering and applied Sciences, Vol. 5, No.5, May 2010
- 2) D.A.B. Zambra, C,Rech, 1.R.Pinheiro, "Comparison of neutral point clamped symmetrical and hybrid asymmetrical multilevel inverter ", IEEE Trans. Ind. Electron., Vo1.57, no.7, pp 2297-2306, July 2010.

- M. Dileep Krishna and Shelly Vadhera, "Application of hybrid multilevel inverter in wind and photo voltaic generating systems", National conference on Recent Trends In Energy, Systems And Control (RTESC-13), pp. 5-9, 15-16 March 2013.
- 4) Nabae, I. Takahashi, and H. Akagi, A new Neutral point- clamped PWM inverter, IEEE Transactions on Industrial Applications, vol.IA-17, No. 5, pp. 518–523,1981.Lijo Jacob et al., A Survey Of Modulation Techniques For A Series Connected Voltage Source Inverters, International Journal of Advanced Engineering Technology, Vol. VII/ Issue II.April-June,2016.
- 5) Amol K. Koshti, M. N.Rao, 'A Brief review on multilevel inverter topologies', 2017 IEEE International Conference on Data Management, Analytics and Innovation (ICDMAI) Zeal Education Society, Pune, India, Feb 24-26, 2017.
- 6) Madhusudhana J, P S Puttaswamy, Harshit Agrawal "A comparative analysis of different multilevel inverters" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE) Vol. 5, Issue 7, July 2016.
- Karthik .KI, Narsimharaju B., Srinivasa Rao S, "Five-Level Inverter Using POD PWM Technique", IEEE 2015, International Conference on Electrical, Electronics, Signals, Communication and Optimization (EESCO) – 2015.
- Sourabh Rathore, Mukesh Kumar Kirar And S. K Bhardwaj, "Simulation Of Cascaded H- Bridge Multilevel Inverter Using Pd, Pod, Apod Techniques", Electrical & Computer Engineering: An International Journal (ECIJ) Vol. 4, Num. 3, Sep. 2015.
- 9) M. Vijeh, M. Rezanejad, E. Samadaei, and K.Bertilsson, "A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View," IEEE Trans. Power Electron., pp. 1–1, 2019.
- 10) K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel Inverter Topologies with Reduced Device Count: A Review," IEEE Trans. Power Electron., vol. 31, no. 1, pp. 135–151, Jan. 2016.
- 11) S. Sabyasachi, V. B. Borghate, R. R. Karasani, S. K. Maddugari, and H. M. Suryawanshi, "Hybrid Control Technique-Based Three- Phase Cascaded Multilevel Inverter Topology," IEEE Access, vol. 5, pp. 26912–26921, 2017.
- 12) E. Babaei, S. Laali, and S. Alilu, "Cascaded multilevel inverter with series connection of novel H-bridge basic units," IEEE Trans. Ind. Electron., vol. 61, no. 12, pp. 6664–6671, 2014.
- 13) M. D. Siddique, S. Mekhilef, N. M. Shah, A.Sarwar, A. Iqbal, and M. A. Memon, "A New Multilevel Inverter Topology With Reduced Switch Count," IEEE Access, pp. 58584–58594, 2019.
- 14) J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," IEEE Transactions on Industry Applications, vol. 49, no. 4, pp. 724-738, Aug. 2002.
- 15) K. B. Bhaskar1, T. S. Sivakumaran, and M. Devi, "Implementation of 11 level cascaded multilevel inverter using level shifting pulse width modulation technique with different loads," IPASJ International Journal of Electrical Engineering, vol. 2, no. 10, pp. 20-31.
- P. K. Dewangan and U.T. Nagdeve, "Review of an inverter for grid connected Photovoltaic (PV) Generation System," International Journal of Scientific & Technology Research, vol. 3,no. 10, October 2014.
- 17) P. Palanivel, S.S. Dash "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation technique" IET Power Electronics vol. 4, no. 8, pp. 951-958,2010.
- 18) Dubey, A. and Bansal, A.K., "Cascade H-bridge multilevel inverter at different Modulation index", International Journal of Scientific and Research Publications, Volume 6, Issue 8, pp. 139-145, 2016.

- 19) Palanivel, P., Dash, S.S.: 'Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques ', IET Power Electron., 2011, 4, (8), pp. 951–958.
- Jagadish Chandra Pati, Jayanta Kumar Sahu, Harmonic Analysis by Using Various PWM Techniques and Their Comparison, International Journal of Advanced Research in Science and Technology, ISSN 2319 – 1783
- R. A. Vargas, A. Figueroa, L. Hernandez and M. A. Rodriguez, "Analysis of Minimum Modulation for the 9-Level Multilevel Inverter in Asymmetric Structure" IEEE Latin America Transactions, vol. 13, no. 9, September 2015
- S. T. Meraj, K. Hasan, A. Masaoud, "A Modified Configuration of Cross-Switched T-Type (CT-Type) Multilevel Inverter," in IEEE Trans- actions on Power Electronics, vol. 35, no. 4, pp. 3688-3696, April 2020.
- 23) Azeem, M.K. Ansari, M. Tariq, A. Sarwar, I. Ashraf, "Design and Modeling of Solar Photovoltaic System Using Seven-Level Packed U-Cell (PUC) Multilevel Inverter and Zeta Converter for Off-Grid Application in India", Electrica vol. 19, no. 2, pp. 101-112, Dec 2019.
- 24) M. Vijeh, M. Rezanejad, E. Samadaei, K. Bertilsson, "A General Re- view of Multilevel Inverters Based on Main Submodules: Structur- al Point of View" in IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9479-9502, Oct. 2019.
- 25) M. Tariq, M. Meraj, A. Azeem, A. I. Maswood, A. Iqbal, B. Chokkalin- gam, "Evaluation of level-shifted and phase-shifted PWM schemes for seven level single-phase packed U cell inverter," in CPSS Transactions on Power Electronics and Applications, vol. 3, no. 3, pp. 232-242, Sept. 2018.
- 26) J.G. Shankar, J.B. Edward, "Design and Implementation of 15-Lev- el Asymmetric Cascaded H Bridge Multilevel Inverter," Journal of Electrical Engineering, vol. 17, no. 2, pp. 396-404, Jun 2017.